REMARKS

Claims 1–36 are pending in the present application.

Claims 1, 10–11, 22 and 24 were amended herein for explication and clarity.

Reconsideration of the claims is respectfully requested.

35 U.S.C. § 112, First Paragraph (Enablement)

Claims 1–36 were rejected under 35 U.S.C. § 112, first paragraph as claiming subject matter that is not described in the specification in a manner enabling one skilled in the relevant art to make or use the claimed invention. This rejection is respectfully traversed.

Any analysis of whether a particular claim is supported by the disclosure in an application requires a determination of whether that disclosure, when filed, contained sufficient information regarding the subject matter of the claims as to enable one skilled in the pertinent art to make and use the claimed invention. MPEP § 2164.01, p. 2100-195 (8th ed., rev. 3, August 2005). The test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation. *Id.* A patent need not teach, and preferably omits, what is well known in the art. *Id.* The Patent Office has the initial burden of establishing a reasonable basis to question the enablement provided for the claimed invention. MPEP § 2164.04 at 2100-197. The minimal requirement for a proper enablement rejection is to give reasons for the uncertainty of the enablement. *Id.*

The Office Action asserts that the recited limitation "a control preventing the memory segments from receiving changes to the data elements contained therein at a rate faster than a transfer rate of memory segments over the data link" is not described in the specification in such a way as to enable one skilled in the relevant art to make and use the claimed invention. However, the specification discloses that when calls are processed, records of the associated call state changes and resource allocations are stored in various records within memory segment 212. Specification, page 28, lines 1–4. Firewire data link controllers 215 format and transfer data according to DMA (data memory access) descriptors stored in locally accessible memory 216. Specification, page 28, line 19 through page 29, line 2. As each record within memory segment 212 is modified and the change is detected, the record is copied into FIFO (first in/first out) queue 213 by DMA circuit 214. Specification, page 29, lines 3–4. Control processor 211 creates or revises a DMA descriptor for each modified record. Specification, page 29, lines 15–17. Preferably, the FIFO queue 213 must be emptied *at least as fast* as the control processor 211 is processing calls (and therefore modifying records within memory segment 212). Specification, page 32, lines 6–9. To accomplish this, a FIFO queue full signal 217 may be needed to control the flow of data into the Firewire data link 230 by allowing the control processor 211 to suspend processing as necessary (*i.e.*, the control processor 211 suspends processing as necessary to prevent memory segments 212 from receiving changes to the data elements contained therein at a rate faster than a transfer rate of memory segments 212 over the data link 230). Specification, page 32, lines 9-12.

In one embodiment of the claimed invention, depicted in Figure 4C and described in relevant part at page 30, line 18 through page 33, line 2 of the specification as filed, changed records within Record 1 through Record x for a memory segment 212 are copied from active component 210 to standby component 20. Specification, page 30, line 18 through page 31, line 4. The changed records are copied by DMA circuit 214 to the FIFO queue 213 within data link controller 215, then asynchronously transmitted from data link controller 215 to data link controller 235. Specification, page 31, line 12 through page 32, line 2. With respect to the asynchronous transmission of changed records, the specification teaches:

> The basic constraint on call processing relative to redundancy is to assure that the FIFO queue is being emptied at least as fast as the control processor 211 is processing calls (and therefore modifying records within memory segment 212). A FIFO queue full signal 217 may be needed to control the flow of data into the Firewire data link 230 by allowing the control processor 211 to suspend processing as necessary. When the control processor 211 suspends processing, the FIFO queue 213 is (at least partially) emptied, preserving all critical memory updates.

Specification, page 32, lines 6–14. Accordingly, in one embodiment of the invention a FIFO queue full signal is employed to suspend processing by control processor 211 within the active component 210 to allow the FIFO queue to empty via asynchronous transmission. Thus FIFO queue full signal 217 serves as a control preventing memory segment 212 from receiving changes to Record 1 through Record x therein resulting from call processor 211 processing associated calls at a rate faster than a transfer rate of memory segments over the data link. While the control processor 211 may process calls (and therefore modify associated records within a memory segment) at a rate that is

instantaneously higher than the transfer rate, suspension of processing by control processor 211 as necessary prevents the overall rate of change to records within the memory segment from being faster than the transmission of those records over the asynchronous link.

Despite the enabling support for the claim limitation objected to, Applicants are availing themselves of this opportunity to eliminate the unnecessary limitation "rate" from the claims.

Therefore the rejection of claims 1–36 under 35 U.S.C. § 112, first paragraph has been overcome.

35 U.S.C. § 112, Second Paragraph (Indefiniteness)

Claims 1–36 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctively claim the subject matter which the Applicants regard as the invention. This rejection is respectfully traversed.

There are two separate requirements under 35 U.S.C. § 112, second paragraph. MPEP § 2171, page 2100-211 (8th ed., rev. 3, August 2005). The first is subjective and requires that the claims must set forth the subject matter that the Applicants regard as their invention. *Id.* The second ("definiteness") requirement is objective and requires that the claims must particularly point out and distinctively define the metes and bounds of the subject matter that will be protected by the patent grant (*i.e.*, whether the scope of the claim is clear to one of ordinary skill in the art). *Id.* The test for compliance with definiteness requirement 35 U.S.C. § 112, second paragraph is whether the claim as a whole apprises one of ordinary skill in the art of its scope. MPEP § 2173.02, page 2100-213.

A rejection under 35 U.S.C. § 112, second paragraph must be accompanied by an analysis as to why the phrase(s) used in the claim is "vague and indefinite." *Id.* at page 2100-214.

Claims 1, 11 and 24 were rejected as being indefinite and confusing for containing the limitation "a control preventing the memory segments from receiving changes to the data elements contained therein at a rate faster than a transfer rate of memory segments over the data link." As noted above, this limitation is fully supported by the specification. Moreover, the Office Action contains no explanation as to why one skilled in the art would have difficulty determining whether a particular system includes a control preventing memory segments from receiving changes to the data elements contained therein at a rate faster than a transfer rate of data elements within the memory segments over the data link. Accordingly, Applicants respectfully request withdrawal of this rejection.

Claims 10, 22 and 35 were rejected as indefinite and confusing for reciting that the data link comprises an "ATM switch." Applicants believe that those skilled in the art would have no particular difficulty determining whether a data link was implemented comprising (i.e., including at least) an ATM switch. Nonetheless, Applicants have availed themselves of this opportunity to broaden claims 10 and 22, which now recite merely that the data link operates in an asynchronous transfer mode.

Therefore the rejection of claims 1–36 under 35 U.S.C. § 112, second paragraph has been overcome.

35 U.S.C. § 102 (Anticipation)

Claims 1–3, 6–8, 11–13, 16–18, 21, 23–26, 29–31 and 36 were rejected under 35 U.S.C. § 102(b) as being anticipated by European Patent Application No. 0 441 087 A1 to *Alalwan et al.* This rejection is respectfully traversed.

A claim is anticipated only if each and every element is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim. MPEP § 2131 at p. 2100-76 (8th ed. rev. 3 August 2005).

Independent claim 1 recites a direct memory access circuit capable of automatically copying memory segments from the memory to a queue without utilizing a processor changing the memory segments. Independent claim 11 similarly recites a direct memory access circuit within each of the active and standby components, the direct memory access circuit within the active component capable of automatically copying memory segments from the memory within the active component to a queue within the active component without utilizing a processor within the active component changing the memory segments within the active component. Independent claim 24 recites automatically copying memory segments from the memory to a queue utilizing a direct memory access circuit without utilizing a processor changing the memory segments. Such features are not found in the cited reference. Data from memory change detector 28 in *Alalwan et al* is written to write-ahead queue (WAQ) 32 in response to execution of an Establish Recovery Point (ERP)

instruction by the processor 12 for the unit 10, and is performed under the direction and control of that processor. *Alalwan et al*, page 6, line 1 through page 7, line 7.

Independent claims 1, 11 and 24 each recite a control preventing the memory segments from receiving changes to the data elements contained therein faster than transfer of data elements within the memory segments over the data link. Such a feature is not found in the cited reference. The cited portion of *Alalwan et al* specifically teaches that the finite state machine controlling copying of memory changes is hard-wired to match the speed at which such memory changes may occur. *Alaiwan*, page 7, lines 50–52. Thus *Alalwan et al* teaches implementing a data transfer system that operates at the same frequency as the processor, rather than controlling the processor to prevent changes from occurring faster than the changed data can be copied by the data transfer system.

Therefore, the rejection of claims 1–3, 6–8, 11–13, 16–18, 21, 23–26, 29–31 and 36 under 35 U.S.C. § 102 has been overcome.

35 U.S.C. § 103 (Obviousness)

Claims 9, 19–20 and 32–34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Alalwan et al* in view of an article by Nagar, et al., "Issues in Designing and Implementing a Scalable Virtual Interface Architecture," IEEE, 2000, pp. 405-412 ("*Nagar*"). This rejection is respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142, p. 2100-133 (8th ed. rev. 3 August

2005). Absent such a *prima facie* case, the applicant is under no obligation to produce evidence of nonobviousness. *Id.*

To establish a *prima facie* case of obviousness, three basic criteria must be met: First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *Id.*

As noted above, independent claims 1, 11 and 24 (from which the rejected claims depend) each recite features not found in *Alalwan et al.* Such features are also not found in *Nagar.*

Therefore, the rejection of claims 9, 19–20 and 32–34 under 35 U.S.C. § 102 has been overcome.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***dvenglarik@davismunck.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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Date: 12-10-05

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